T.E. Sem - VI (ECS) (C-Scheme) Dec. 2025 16/12/2025

(3 Hours) [Total Marks: 80]

N.B.: (1) Question No. 1 is **Compulsory**.
(2) Attempt any **three** questions out of the remaining **five**.
(3) Each question carries 20 marks and sub-question carry equal marks.
(4) Assume suitable data if required.

1. Solve **any 4**
   (a) Explain issues in Hardware Software Co-Design. (5)
   (b) Explain various functions of RTOS kernel. (5)
   (c) Define Inter process Communication. (5)
   (d) Explain use of waterfall model in the design of an embedded system. (5)
   (e) Examine significance of Thumb-2 instructions of Cortex-M3 architecture (5)

2. (a) What is Interrupt latency? List the causes of Interrupt latency and mention methods to minimize latency. (10)
   (b) Decide whether the tasks are schedulable by Necessary and sufficient condition in an embedded system with 4 different tasks with task IDs T1, T2, T3, T4 and estimated completion time 4, 5,6 and 7 mS respectively. T1, T2, T3 and T4 have their cycle duration as 26,32, 20 and 50 ms respectively. (10)

3. (a) Explain features, working and use of CAN Bus Protocol. (10)
   (b) Draw and explain waterfall model used in embedded product design life cycle (EDLC) (10)

4. (a) Explain with example the necessary and sufficient condition of task schedulability. (10)
   (b) Explain briefly interrupt and exception handling in Cortex-M3 architecture. What is NVIC? (10)

5 (a) What is priority inversion problem? Suggest the solution used for the same. Explain bounded and unbounded priority inversion. (10)
   (b) Design a suitable program model to design seat belt warning system for a four wheeler. (10)

6. Write short notes on (any two): (20)
   a. Hardware Testing Tools
   b. Rate Monotonic Scheduling
   c. RS 232 and RS 485 communication interface
   d. Zig-bee and Bluetooth
